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NITRIDED STI LINER OXIDE FOR REDUCED CORNER DEVICE IMPACT ON VERTICAL DEVICE PERFORMANCE

Abstract

A method of fabricating an integrated circuit device comprises etching a trench in a substrate and forming a dynamic random access memory (DRAM) cell having a storage capacitor at a lower end and an overlying vertical metal oxide semiconductor field effect transistor (MOSFET) comprising a gate conductor and a boron-doped channel. The method includes forming trenches adjacent the DRAM cell and a silicon-oxy-nitride isolation liner on either side of the DRAM cell, adjacent the gate conductor. Isolation regions are then formed in the trenches on either side of the DRAM cell. Thereafter, the DRAM cell, including the boron-containing channel region adjacent the gate conductor, is subjected to elevated temperatures by thermal processing, for example, forming a support device on the substrate adjacent the isolation regions. The nitride-containing isolation liner reduces segregation of the boron in the channel region, as compared to an essentially nitrogen-free oxide-containing isolation liner.